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The data processing system has a host sub-system with a host processor, volatile and non-volatile memory devices with image memory structures formed of transfer memory structures. A remote communication interface is connected to the host processor. Portable devices contain data processors with communication interfaces and volatile memories each of structures corresponding with an image structure of the host memory.

The host interface transmits a time signal to establish a communication link with a portable device, and transmits associated structure contents after receiving data entered via a user interface on the portable device. Processing of the received data is monitored and the link is disconnected when it is complete.

ADVANTAGE - Can handle large amounts of data in single communication session. Maintains data integrity. Minimises time required for sessions, reducing telecommunication costs.

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(54) Title A data processing system

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"A Data Processing System"

The invention relates to a data processing system of the type which has users who are located remotely from each other and from a host part of the system, and more particularly to a situation where many of the users are travelling from place to place.

Clearly, satisfactory operation of such a system is dependent entirely on data integrity. In the particular circumstances under which such a type of system operates, problems can very easily arise in communication of data from the portable data processors to the host sub-system. Very often, problems can arise for very simple reasons such as battery power going low during a communications session. There may be very simple occurrences of human error to cause problems such as accidental pressing of incorrect keys on the keyboard, or incorrect settings of a modem.

British Patent Specification No. GB-B-2 168 515 (C.T. Farley) describes a communication and data processing system having a number of portable units and a central control unit. On transmission of data from a portable unit, the central control unit discriminates between data of different categories and then processes the data. Undoubtedly, this system operates very effectively in restaurants and other similar situations. However, it would appear not to be suitable for other uses where there is a requirement for much more data to be processed such as in a nationwide food distribution company where orders may be inputted for very large quantities of goods at any one communication session.

United States Patent Specification Nos. US-A-5,050,207 and US-A-5,157,717 (National Transaction Network Inc.)

describe portable automated teller machines for use in a financial institution environment. Features are provided for ensuring security of data which is communicated. However, while these systems are also apparently effective for the requirements of financial institutions, they do not incorporate technical features to solve the above-mentioned problems.

According to the invention, there is provided a data processing system comprising:

a host sub-system comprising:

a host processor;

a non-volatile memory device having a plurality of image memory structures, each comprising a transfer memory structure;

an interface connected to the host processor and being constructed for remote communications; and

a volatile memory device,

a plurality of portable devices, each comprising a data processor connected to an interface constructed for remote communications, each data processor comprising a non-volatile memory structure corresponding to an image memory structure of the host sub-system and comprising a volatile memory device,

means in the host sub-system interface for automatically downloading a time signal to a portable device when a communications link is established, for automatically transmitting contents of the transfer structure of the associated image memory structure

after receipt and acknowledgement of upload data from the portable device, for monitoring processing of the host processor with the received data, and for disconnecting the communications link when such processing is complete; and

means in the interface of each portable device for establishing a communications link with the host sub-system, for automatically synchronising a real-time clock on receipt of the time signal from the host sub-system, for transmitting data received from an operator input interface as upload data to the host sub-system, and for monitoring input ports for an acknowledgement signal from the host sub-system.

In one embodiment, the interfaces of the portable devices and of the host sub-system each comprise means for transmitting and receiving data under a packetising protocol.

Preferably, the interfaces comprise means for defining a pair of structures in volatile memory to act as communication buffers, and means for directing data transmission by:-

writing a data packet to a first buffer;

transmitting the data packet from the first buffer;

writing a data packet to a second buffer;

transmitting the data packet from the second buffer;

monitoring input ports for receipt of an acknowledgement signal for the first packet; and

writing a fresh packet to the first buffer and transmitting it after receipt of a satisfactory acknowledgement signal.

In another embodiment, each portable processor and the host processor are connected to a counter and comprise means for setting a maximum count for the number of packet transmission attempts.

Ideally, the interface of each portable device is connected to a modem, in turn connected to an acoustic coupler.

In a still further embodiment, the host processor comprises means for periodically monitoring write operations to the image memory structures, and means for automatically writing update data to the corresponding transfer structure.

Preferably each portable data processor comprises means for maintaining a marker data segment in the non-volatile memory device indicating current processing activity for future rollback.

Ideally, the marker is a file header written to a file allocation table of the non-volatile memory device.

The invention will be more clearly understood from the following description of some embodiments thereof, given by way of example only with reference to the accompanying drawings in which:-

Fig. 1 is a schematic representation of a data processing system of the invention;

Fig. 2 is a flow chart illustrating the initialisation operations of the system; and

Fig. 3 is a flow chart illustrating the manner in which communications and subsequent data processing operations are carried out.

Referring to the drawings, there is shown a data processing system of the invention. The system comprises a set of portable devices 1 of the type which are commonly referred to as "Notebooks". They have the full capability of microcomputers and include a data processor 2(a), 2(b) etc., a fixed disk non-volatile memory device, and a volatile memory circuit. Each portable processor 2 is connected to a modem and acoustic coupler 3(a), 3(b) etc. Thus each portable processor 2 may be used for communication of data to the remainder of the system using a conventional telephone, if required.

Fig. 1 also illustrates the part of the system 1 located at the central control site, referred to as a host sub-system 10. The sub-system 10 comprises a host processor 11 which is of the mainframe type and which includes non-volatile memory devices, namely fixed disks. The disks store a pre-defined memory structure 12(a), 12(b), etc. associated with each portable processor 2. For example, the memory structure 12(a) is associated with the portable processor 2(a). In addition, there is a set of internal transfer memory structures 13, the structure 12(a) having a transfer structure 13(a), the structure 12(b) having a transfer structure 13(b) etc.

The host processor 11 is also connected to a remote communications interface 14 which directs all of the remote communications and this is connected to a memory circuit which is controlled to form a pair of packet

buffer memories 15 and 16 and a counter 17. This memory is volatile. The interface 14 is also constructed to form a serial transmit queue 18 in the volatile memory circuit. While the items 15, 16, 17 and 18 are defined in terms of operation of the interface 14 as they are temporarily stored during data processing operations on the volatile memory circuit, they could just as easily be separate memory circuits dedicated for the particular purpose. For example, the serial transmit queue 18 could comprise a dedicated set of video random access memories (VRAMs) which are particularly suitable as they have a shift register for fast serial communication. The portable processors 2 each include an interface similar to the remote communications interface 14.

The system 1 is initialised as illustrated in Fig. 2 by the host sub-system 10 recording parameter data 21 associated with each of the portable processors 2. This parameter data includes specifications of the nature of the data which is to be stored in each portable processor, and the nature of the data updates transmitted from the portable processor. In step 22 the host processor 11 defines the image memory structure 12 which is associated with the portable processor 2 and in step 23 it defines the transfer memory structure 13 within the image memory structure 12. Although it appears from the diagram of Fig. 1 that the image and transfer memory structures 12 and 13 are identical, this is not necessarily the case as each portable processor has its own processing requirements and the image structure 12 directly reflects the permanent data storage structure of the associated portable processor 2. For this reason, the transfer memory structures 13 may also be different because they are generated in step 23 to be suitable for storage of data which is to be downloaded from the host sub-system 10 to the associated portable processor 2. The size and

nature of the structure is thus a function of the image memory structure 12 generated in step 22. The term "image" is used because the structure 12 is in direct correlation to the non-volatile storage structure of the associated portable processor 2. In practice there will be many portable processors 2 and for clarity, only three are illustrated.

In step 24 of the process 20, the host processor 11 writes initialisation data to the image memory structure 12 of the new portable processor 2. This data is the data which is also written to the particular portable processor 2 as illustrated by the step 25 of the process 20. The initialisation process 20 is repeated for each additional portable processor, and once initialised the image structures remain on a permanent basis and may be regarded as being hard-coded.

Each processor 2(a), 2(b), etc is constructed to monitor the data which is inputted at the keyboard by the operator. In more detail, the processor monitors events which generate a trigger which causes it to automatically write a marker to the non-volatile memory device. These events include the updating of a new set of data in the memory device, the input of a command for communication with the host sub-system 10 or any other important event. These events are driven by the operator inputting signals at the keyboard. The form of the marker is a file header which is written to the file allocation table of the storage device. Another important aspect of operation of the portable processors 2 which ensures data integrity is the fact that updates take place to the non-volatile memory device on an atomic basis only. Prompts are automatically generated for user inputting of a complete set of data if an inputting session is interrupted such as by a low battery status or by accidentally switching off

the machine. The manner in which this is implemented is that the processor does not record addresses for subsequent access to portions of the disk which have been written to during portion of a data update. Accordingly, while the data is stored it may not be accessed and a complete inputting session is required for the particular set of data.

A very important aspect of the system is the manner in which data is uploaded from the portable processors 2 to the host sub-system 10 in a manner which ensures integrity of the data. As with many data communications systems the modem 18 incorporates error-correction facilities. However, to supplement the operation of the modem 19 and the modem connected to the couplers 3, the interface 14 and the interface, not shown, of the each of the portable processors 2 are constructed to operate so that data is communicated in a reliable and relatively error-free manner. The manner in which a communications session is executed is illustrated by the process 30 of Fig. 3. In step 31 a portable processor 2 opens a communications link with the host sub-system 10. Immediately upon receipt of the connection signal, the interface 14 of the host sub-system 10 transmits a time signal after reference to its clock. In step 33, the time signal is received by the interface of the relevant portable processor 2 and it automatically synchronises its real-time clock with the host sub-system 10. These operations are automatic and ensure synchronisation for all communication sessions.

As indicated by step 34, the portable processor output interface then transmits upload data is which is all of the data which has been inputted at the keyboard. An example is sales order data where the operator is a sales representative. As stated above, the portable processor 2 incorporates an interface which is constructed to

control memory to provide arrangements similar to the buffers 15 and 16, the counter 17 and the serial transmit queue 18 which are illustrated in Fig. 1 for the host sub-system 10. For the portable processor 2 to transmit upload data in step 34, it writes a packet of data to the first buffer. Building of the data packet involves retrieval of the first 128 bytes of the data and inserting a correct sequence number into the packet. A checksum is then calculated and is appended to the last character, namely, character number 132 of the packet. The counter is then set to zero and the packet from the first buffer is written to the serial transmit queue. The packet is then transmitted via the modem 3 and the interface awaits an acknowledgement from the host sub-system 10. A packet is then written to the second buffer and is then transmitted. The first buffer is refreshed with the third packet when the acknowledgement is received for the first packet, and so on. If a return signal is received from the host sub-system 10 to indicate that the packet has not been satisfactorily received (for example, the check sum is incorrect) the value in the counter is incremented and the packet is re-transmitted. The output interface had previously set a maximum number of attempts and re-transmission takes place until the maximum set number is reached. An important aspect of the invention is the fact that both the portable processor 2 and the host sub-system 10 are constructed in a similar manner for communications. The interface at the host sub-system 10 verifies the packet received into the first buffer and transmits an acknowledgement. It then verifies the packet in the second buffer.

When all of the upload data has been transmitted from the portable processor 2, an acknowledgement (end-of-transmission) signal is transmitted in step 35 from the output interface 14 of the host sub-system 10. During the

steps 31-35, the host processor 11 had been operating in parallel to retrieve data from the transfer memory structure 13 associated with the particular portable processor 2. As illustrated by the arrows A, the transfer structure 13 is updated on an in-line basis after data updates have taken place to the image memory structure 12. Thus, whenever a connection is established by a portable processor 2, the data which is to be downloaded by the host sub-system 10 is already stored in the non-volatile memory 13 and is ready for retrieval. It is that data which is written by the host processor 11 to the volatile memory circuit. In step 36 the host processor transmits this download data via the serial transmit queue 18 in the manner previously described for the portable processor 2. Once this has been safely received and acknowledged, the host processor 11 clears the transfer structure 13.

Ending of the communications sessions is quite important as when it is done correctly it ensures that all data has been safely communicated. Accordingly, this is carried out by the portable processor 2 transmitting a final indicator in step 38 to the host sub-system 10 to indicate that no further upload data is to be transmitted and also that no download data in addition to what has already been transmitted is required. The host processor 11 monitors the interface 14 for receipt of this signal and continues with the necessary data processing updates which are carried out using the received upload data. When the next stage of data processing has been initiated, and the host processor does not require any further data, it disconnects the communications link in step 40. By disconnecting the communications link in this manner the problems of delays which are caused by further processing of the host processor 11 are avoided.

It will be appreciated that by the manner in which the portable processors operate, there can be immediate roll-back to a previously confirmed memory status by use of the marker file headers. Further, because updating is carried in an atomic manner, data integrity is maintained. Further, the manner in which the communications sessions are carried out help to ensure that they are not only carried out with data integrity, but are carried out efficiently with relatively little time being required. It has been found, for example, that where 300 kB of data is being uploaded and approximately 100 kB being downloaded, the communications session takes no longer than 70 seconds. Over a period of time for operations of a distribution company, this causes a significant reduction in telecommunications cost.

The invention is not limited to the embodiments hereinbefore described, but may be varied in construction and detail.

disconnecting the communications link when such processing is complete; and

means in the interface of each portable device for establishing a communications link with the host sub-system, for automatically synchronising a real-time clock on receipt of the time signal from the host sub-system, for transmitting data received from an operator input interface as upload data to the host sub-system, and for monitoring input ports for an acknowledgement signal from the host sub-system.

2. A system as claimed in claim 1, wherein the interfaces of the portable devices and of the host sub-system each comprise means for transmitting and receiving data under a packetising protocol.

3. A system as claimed in claim 2, wherein the interfaces comprise means for defining a pair of structures in volatile memory to act as communication buffers, and means for directing data transmission by:-

writing a data packet to a first buffer;

transmitting the data packet from the first buffer;

writing a data packet to a second buffer;

transmitting the data packet from the second buffer;

monitoring input ports for receipt of an acknowledgement signal for the first packet; and

writing a fresh packet to the first buffer and transmitting it after receipt of a satisfactory acknowledgement signal.

4. A system as claimed in claims 2 or 3, wherein each portable processor and the host processor are connected to a counter and comprise means for setting a maximum count for the number of packet transmission attempts.

5. A system as claimed in any preceding claim, wherein the interface of each portable device is connected to a modem, in turn connected to an acoustic coupler.

6. A system as claimed in any preceding claim, wherein the host processor comprises means for periodically monitoring write operations to the image memory structures, and means for automatically writing update data to the corresponding transfer structure.

7. A system as claimed in any preceding claim, wherein each portable data processor comprises means for maintaining a marker data segment in the non-volatile memory device indicating current processing activity for future rollback.

8. A system as claimed in claim 7, wherein the marker is a file header written to a file allocation table of the non-volatile memory device.

9. A system substantially as hereinbefore described with reference to and as illustrated in the accompanying drawings.

1/3 (FORMAL)

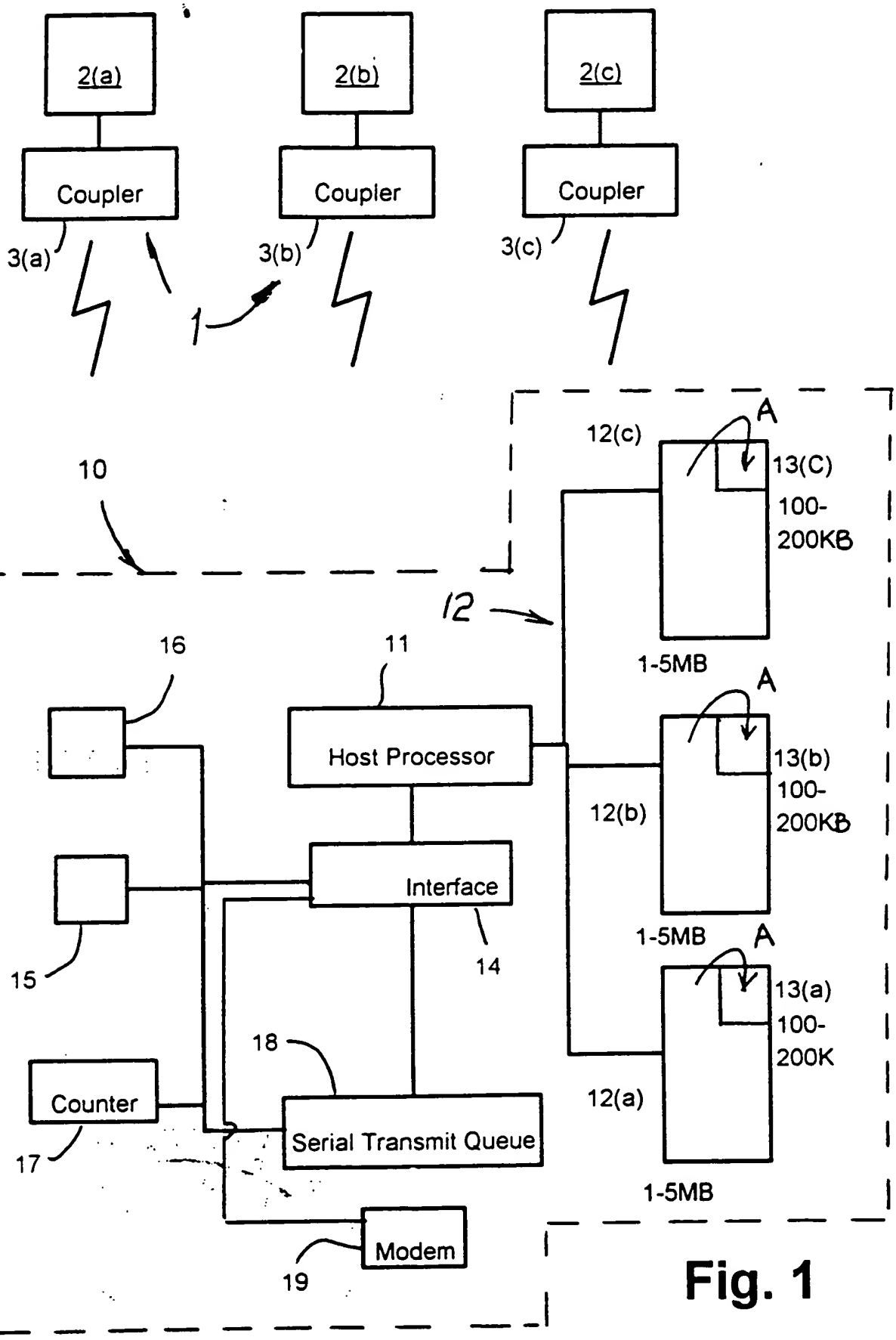

Fig. 1

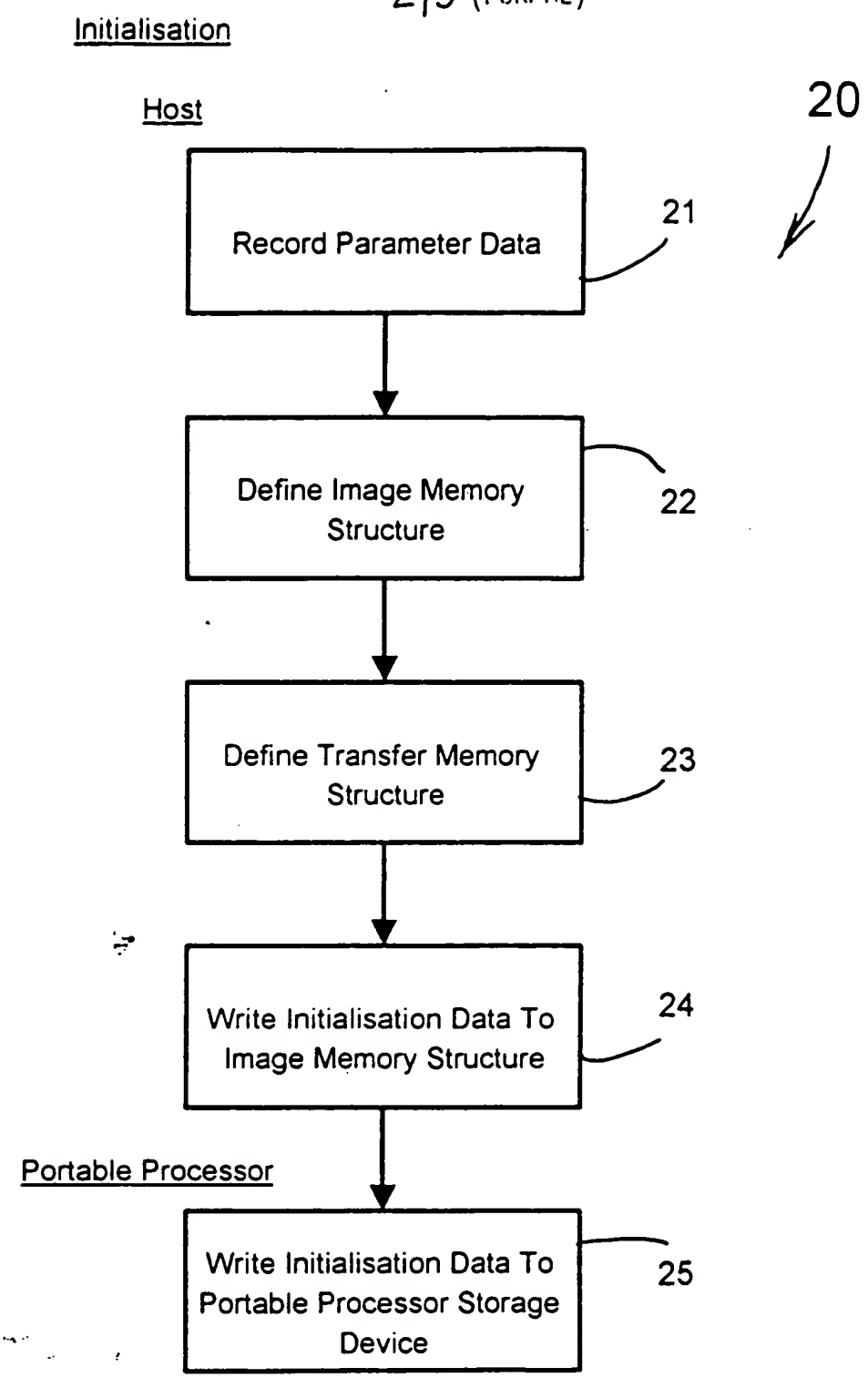
Initialisation
Host
20
Record Parameter Data
21
Define Image Memory Structure
22
Define Transfer Memory Structure
23
Write Initialisation Data To Image Memory Structure
24
Portable Processor
Write Initialisation Data To Portable Processor Storage Device
25

Fig. 2

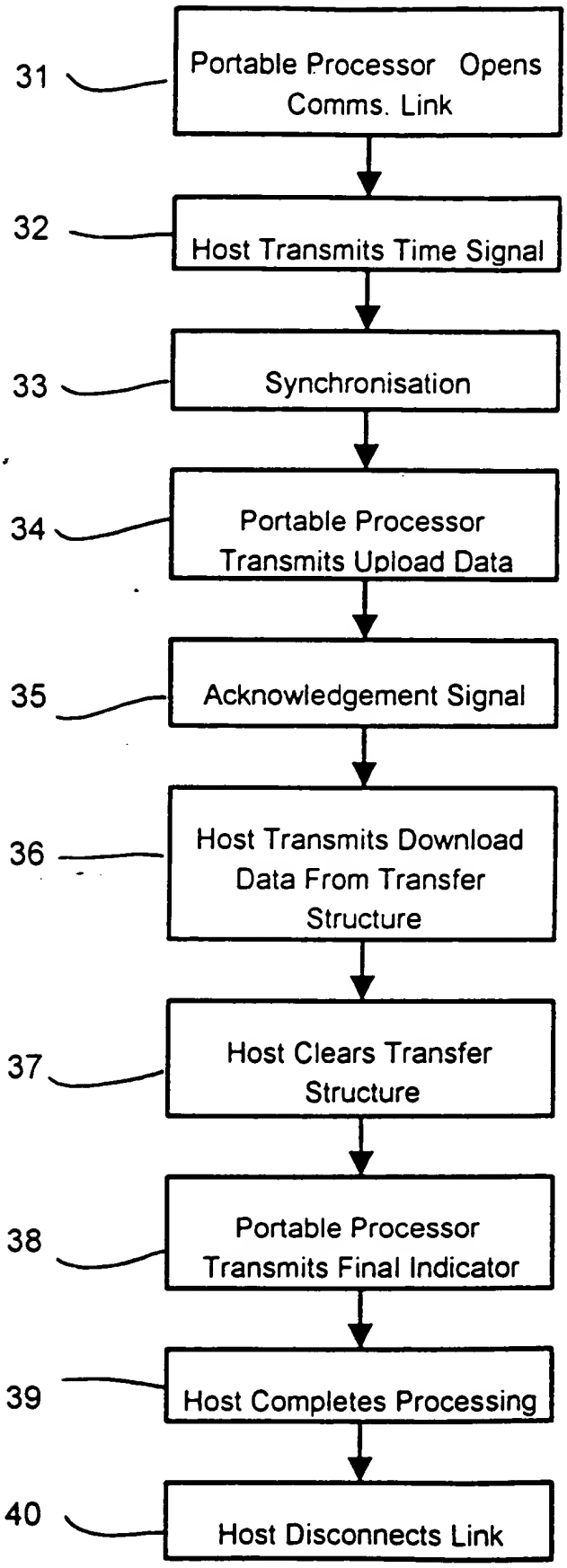
31
Portable Processor Opens Comms. Link
30
32
Host Transmits Time Signal
33
Synchronisation
34
Portable Processor Transmits Upload Data
35
Acknowledgement Signal
36
Host Transmits Download Data From Transfer Structure
37
Host Clears Transfer Structure
38
Portable Processor Transmits Final Indicator
39
Host Completes Processing
40
Host Disconnects Link

Fig. 3